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Design and simulation of a nanoelectronic single-electron universal Control–Control-Not gate

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Abstract

A single-electron universal Control–Control-Not gate (CCN gate) is presented in this paper. Bits of information are represented by the presence or absence of single-electrons at conducting islands. The logic operation of the CCN gate as well as its XOR, AND, NAND and NOT operation is verified using simulation. The stability of its universal operation is analysed using a Monte Carlo method. Stability analysis using free energy diagrams and stability plots verify the correct and stable operation of the gate.
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Keywords: Nanoelectronics; Single-electronics; Control–Control-Not gate

1. Introduction

Single-electron tunnelling (SET) devices exploit effects that arise due to the quantized nature of charge. Therefore, single-electron technology deals with the control of transport and position of a single-electron or a small number of electrons. The fundamental physical principle of single-electronics is the tunnelling effect through a Coulomb blockade, which has been observed and studied by Gorter [1]. The small size and low power dissipation of single-electron circuits makes them potentially useful for logic and memory circuits [2,3]. Single-electronics is one of the emerging nanoelectronic technologies [4].

Although single-electron circuits are expected to operate at room temperature when the island size is reduced to about 10 nm [3], several single-electron circuits have recently been proposed in the literature: inverters and, pumps [5,6], majority gates [7,8], logic gates [9–11], half-adders [12] and random access memory arrays [13]. Computer-aided design and simulation is an indispensable tool for the study and analysis of single-electron circuits. Several simulators have been implemented to support single-electron circuit design and fabrication [14–18].

The Control–Control-Not (CCN) gate has three inputs and three outputs. The first and the second output take the logic values of the first and second input, respectively. If the first and the second input have both the logic value '1', the third output takes the complementary value of the third input. In all other cases, the third output takes the logic value of the third input. The CCN gate is a computationally universal gate, i.e. any Boolean function can be implemented using only CCN gates.

A single-electron CCN gate would be very useful, because digital single-electron circuits that use only one type of gate would be very much easier to fabricate than single-electron circuits that use various types of gates. The aim of this work is to show that a single-electron universal CCN gate is possible.

A single-electron CCN gate has been designed and simulated using SIMON. SIMON is a single-electron circuit simulator based on a Monte Carlo method [18]. The universality and the stable operation of this gate have been verified.

The necessary background in single-electronics is given in Section 2. The conventional CCN gate, its symbol and truth table are presented in Section 3. The single-electron CCN gate circuit and its operation are described in Section 4 and its stability is studied and analysed in Section 5. The universality of the single-electron CCN gate is shown in Section 6 and the conclusions are drawn in Section 7.

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2. Single-electronics

2.1. Coulomb blockade

The basic concept of single-electronics is the Coulomb blockade. Consider an electroneutral small conductor, which is called an island. The island has exactly as many electrons as it has protons in its crystal lattice. The electroneutral island does not generate any appreciable electric field beyond its borders and a weak external force can bring an additional electron from outside into the island [3].

Now the net charge, Q, of the island is $-e$, where e is the elementary charge. The energy E_c required to charge an island with an electron is called Coulomb energy and is given by:

$$E_c = \frac{e^2}{2C_i} \tag{1}$$

where C_i is the capacitance of the island. Although the extra charge $-e$ in the island is very small, the electric field generated by this charge is inversely proportional to the square of the island size and may become very strong in nanoscale structures. If the island is a 10 nm sphere in vacuum, the field is as large as 140 kV/cm [3]. This strong electric field inhibits further electron transfer into the island, thus giving rise to the Coulomb blockade effect. Single-electronics exploit Coulomb blockade by representing bits of information by the presence or absence of a single-electron or a small number of electrons in conducting islands.

To keep an extra electron confined into an island, the Coulomb energy should be greater than the thermal energy otherwise, thermal fluctuations may drive the electron outside the island. Thus, the necessary condition is:

$$E_c = \frac{e^2}{2C_i} > k_B T \tag{2}$$

where k_B is Boltzmann's constant and T is the absolute temperature. Eq. (2) gives the lower theoretical limit for the Coulomb charging energy E_c. However, most current single-electron circuits comprise devices that require much higher values of this energy ($\sim 100 k_B T$) in order to avoid thermally induced random tunnelling events [3].

2.2. Single-electron circuits

Single-electron circuits consist of conducting islands, tunnel junctions, capacitors, and voltage sources. The islands are arbitrarily connected with tunnel junctions, capacitors and voltage sources. Electrons tunnel independently from island to island through tunnel junctions. To assure that electron states are localized in the islands, all tunnel resistances must be larger than the fundamental resistance R_q :

$$R > R_q = \frac{\hbar}{e^2} \cong 25,813\ \Omega \tag{3}$$

where $\hbar$ is Planck's constant.

To simulate the tunnelling of electrons from island to island in a single-electron circuit one has to determine the rates of all possible tunnel events. The tunnel rate of a possible tunnel event depends on the change in the circuit's free energy caused by this particular event [3,18]. The free energy, F, of a single-electron circuit is the difference between the electrostatic energy, U, stored in its capacitances and the work done by the voltage sources of the circuit, W :

$$F = U - W \tag{4}$$

The electrostatic energy is given by:

$$U = \frac{1}{2}(q, v)\begin{pmatrix} V \\ Q \end{pmatrix} \tag{5}$$

where q and v are the unknown part of the island charge and voltage matrices, respectively, and Q and V are the known part of the island charge and voltage matrices, respectively. The work done by the voltage sources is given by:

$$W = \sum_n \int V_n(t) i_n(t) \mathrm{d}t \tag{6}$$

where $V_n(t)$ is the voltage of the nth voltage source, and $i_n(t)$ is the current through the nth voltage source.

The tunnel rate, Γ, for a particular tunnel event is given by:

$$\Gamma = \frac{\Delta F}{e^2 R_T\left(1 - \exp\left(-\frac{\Delta F}{kT}\right)\right)} \tag{7}$$

where ΔF is the change in free energy caused by this particular tunnel event, R_T, is the tunnel resistance of the tunnel junction through which the electron is transported, and kT is the thermal energy (k is Boltzmann's constant, and T the temperature). Once the tunnel rates for all possible tunnel events are known the actually occurring event is determined using a Monte Carlo method combined with an exponential distribution of tunnel events [18]. The time duration of a particular tunnel event is given by:

$$\Delta t = -\frac{\ln(r)}{\Gamma} \tag{8}$$

where r is an evenly distributed random number in the interval [0,1]. Among all possible tunnel events, the event with the shortest time duration takes place [3,18].

3. The conventional Control–Control-Not gate

The conventional CCN gate has three inputs and three outputs. The graph of the CCN gate is shown in Fig. 1.

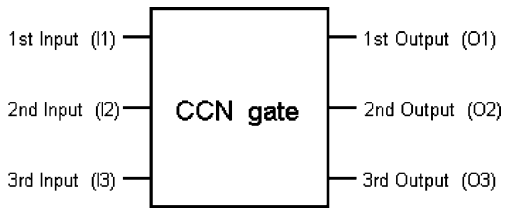

Fig. 1. The graph of the CCN gate.

Table 1
Truth table of the CCN gate

Input 1	Input 2	Input 3	Output 1	Output 2	Output 3
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

The truth table of the CCN gate is shown in Table 1. The first output and the second output O1 and O2 always take the logic values of the first input and second input I1 and I2, respectively. The third output O3 takes always the logic value of the third input I3, except for the case when I1 and I2 both take the logic value 1. In this case, the third output takes the complementary value of the third input. The CCN gate is a universal gate, i.e. it can operate as a XOR, AND, NAND or NOT gate provided that we set one or two of its inputs at a specific logic value. Therefore, any Boolean function can be implemented using only CCN gates.

If I1 is kept at logic 1, the CCN gate operates as a XOR gate. The inputs of the XOR gate are I2 and I3 and the output is taken from O3. The same thing happens if I2 is kept at logic 1. In this case I1 and I3 are the inputs and O3 is the output. If I3 is kept at logic '0' the CCN gate operates as an AND gate. The inputs of the AND gate are I1 and I2 and the output is taken from the O3. Similarly, if I3 is kept at logic 1, the CCN gate operates as a NAND gate with inputs I1 and I3 and O3 as output. Finally, if I1 and I2 are both kept at logic 1, the CCN gate operates as a NOT gate. The input of the NOT gate is I3 and the output is taken from O3.

4. The single-electron Control–Control-Not gate

4.1. The single-electron circuit

A single-electron CCN gate is a single-electron logic circuit that has the same logic operation as the classical CCN gate but it is constructed using single-electron circuitry.

The circuit of the single-electron CCN gate is shown in Fig. 2. The circuit comprises eight islands $N1-N8$. The islands $N6-N8$ are the output islands. $N6$ is the first output, $N7$ is the second output, and $N8$ is the third output. Twelve junctions $J1-J12$ bound the islands. The capacitances and the resistances of all junctions are shown in Table 2. Junctions $J10-J12$ are less transparent, in order to prevent electron transport from the ground (Vss) to islands $N6-N8$ and vise versa. The voltage source Vdd is constant and its value is 0.1 V.

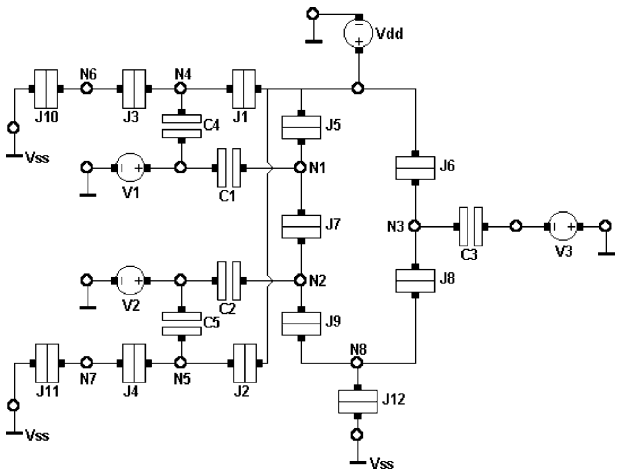

Fig. 2. The circuit of the single-electron CCN gate.

The voltage sources $V1$, $V2$ and $V3$ are the first, the second and the third input of the CCN gate, respectively. These input voltages can take only two values: -60 mV, which corresponds to the logic 0, and 105 mV, which corresponds to the logic 1. The input voltage $V1$ is applied to islands $N1$ and $N4$ through the capacitors $C1$ and $C4$, respectively. The input voltage $V2$ is applied to islands $N2$ and $N5$ through the capacitors $C2$ and $C5$, respectively. Finally, the input voltage $V3$ is applied to island $N3$ through the capacitor $C3$. The capacitors $C1$ and $C2$ have a capacitance of 10^{-18} °F, the capacitors $C4$ and $C5$ have a capacitance of 1.05×10^{-18} °F, and the capacitor $C3$ has a capacitance of 0.8×10^{-18} °F. The output signals of the CCN gate are taken from islands $N6$, $N7$, and $N8$, which are the first, the second and the third output, respectively. The presence of positive

Table 2
Resistances and capacitances of tunnel junctions of the single-electron CCN gate

Tunnel junction	Resistance (Ω)	Capacitance (10^{-18} °F)
$J1$	10^5	1
$J2$	10^5	1
$J3$	10^5	1
$J4$	10^5	1
$J5$	10^5	1.1
$J6$	3×10^4	2.7
$J7$	10^5	2.2
$J8$	3×10^4	0.6
$J9$	10^5	2.5
$J10$	10^8	1.29
$J11$	10^8	1.29
$J12$	10^8	1.46

charge in the output islands corresponds to logic 1, whereas no charge corresponds to logic 0.

4.2. Gate operation

The logic operation of the single-electron CCN gate is shown in Figs. 3 and 4. Fig. 3(a)–(c) shows the time variation of the input voltages $V1$, $V2$, and $V3$, respectively. The inputs are piece-wise constant and apply all possible combinations of logic 0 and 1 to the gate. Fig. 4(a)–(c) shows the time variation of the charge $Q6$, $Q7$ and $Q8$ in the output islands $N6$, $N7$, and $N8$, respectively. The results from the graphs of Figs. 3 and 4 compose the truth table of the single-electron CCN gate, which is identical to that of a conventional CCN

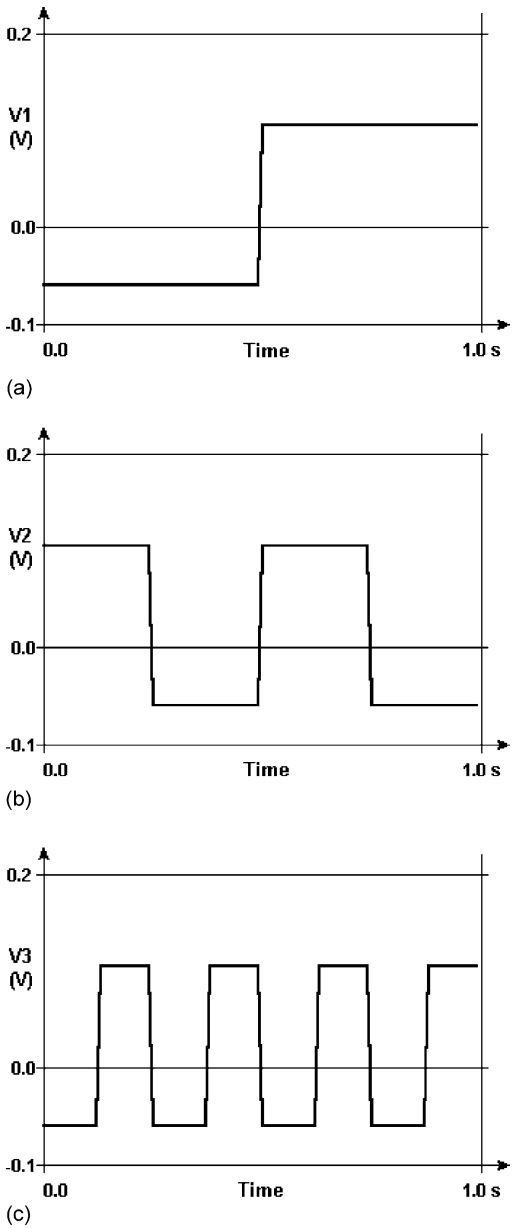

Fig. 3. Input voltages of the CCN gate. (a) Time variation of voltage $V1$, (b) time variation of voltage $V2$ and (c) time variation of voltage $V3$.

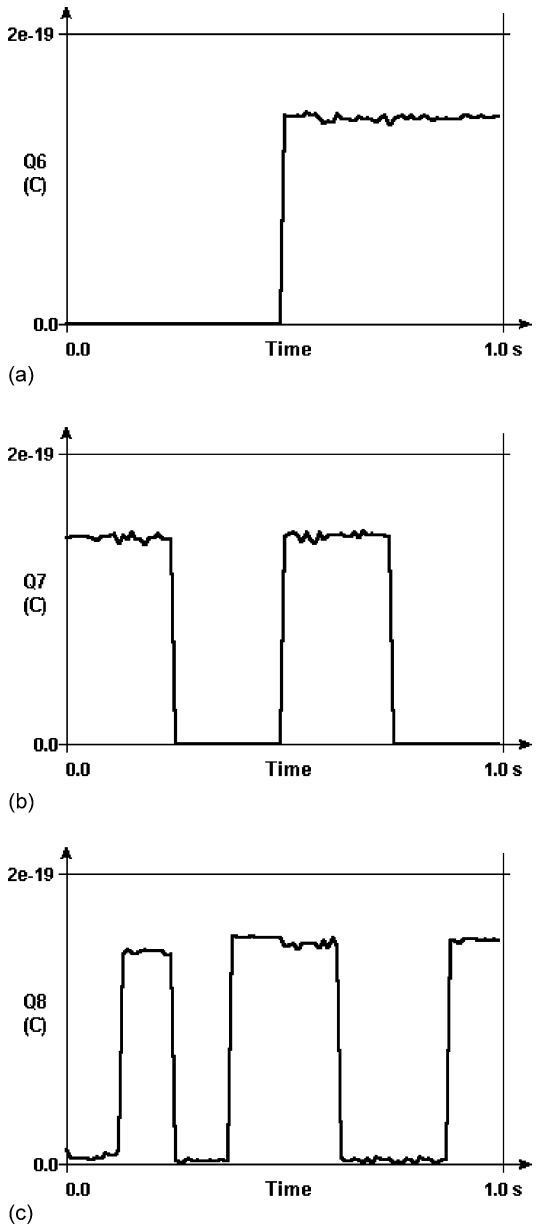

Fig. 4. Output signals of the CCN gate. (a) Time variation of the charge in the island $N6$, (b) time variation of the charge in the island $N7$, and (c) time variation of the charge in the island $N8$.

gate shown in Table 1. The output transition from logic 0 to logic 1, and vice versa, does not drive the circuit to instability. The presence of charge in the output islands can be detected and transferred to circuits connected to the single-electron CCN gate output using a sense amplifier [3].

5. Stability of the single-electron Control–Control-Not gate

The stability of a single-electron circuit is studied by constructing its free energy history diagrams and its stability plots.

5.1. Free energy history diagrams

The free energy history diagrams are used to verify the stable operation of the single-electron CCN gate. The free energy of the circuit is calculated at each step of the path of an electron, starting from ground, an island, or a voltage source, and ending in ground, an island or a voltage source. The calculations were performed using SIMON. The results can be plotted as graphs of energy versus time, or time steps.

The change in circuit free energy during the output transition from 0 to 1, and vise versa, has been calculated and the free energy history diagram of the CNN gate circuit is shown in Fig. 5. Fig. 5(a) shows the transition associated with the first output, where the electron is transported from $N6$ to Vdd through $J3$ and $J1$ leaving, thus, a positive charge in $N6$, and changing the value of the first output from 0 to 1, and vice versa. Initially, there is no extra charge in $N6$ and the free energy is zero. During the second time step, an electron is transported from island $N6$ to island $N4$ through $J3$ and the free energy increases. During the third time step, the electron is transported from island $N4$ to Vdd through $J1$ and there is a significant decrease in the free energy. At this point, the output island $N6$ is positively charged and we have a transition from 0 to 1. The transition from 0 to 1 of the second output produces the same free energy diagram.

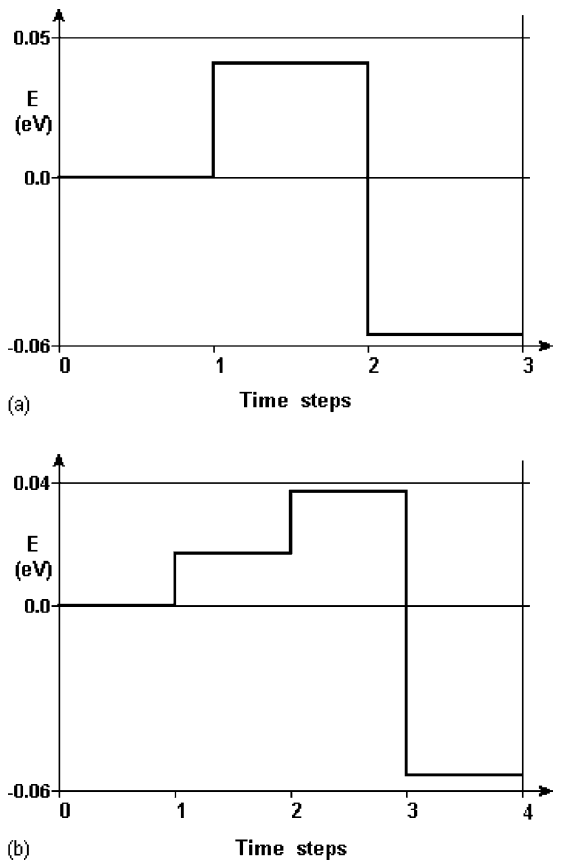

Fig. 5. Free energy history diagrams of the CCN gate circuit. (a) Transition from output island $N6$ to Vdd and (b) transition from output island $N8$ to Vdd.

Fig. 5(b) shows the transition associated with the third output, where the electron is transported from $N8$ to Vdd through $J9$, $J7$ and $J5$ leaving, thus, a positive charge in $N8$ and changing the value of the third output from 0 to 1. Initially, there is no extra charge in $N8$. During the second time-step, an electron is transported from island $N8$ to island $N2$ through $J9$ and the free energy increases. During the third time-step, the electron is transported from island $N2$ to island $N1$ through $J7$ and the free energy increase again. Finally, during the fourth time-step, the electron is transported from $N1$ to Vdd through $J5$ and the free energy decrease significantly. At this point, the output island $N8$ is positively charged and we have a transition from 0 to 1.

Both states (logic 0 and logic 1) of all three outputs correspond to energy minima. This is a strong indication of gate stability, because electrons have to overcome energy barriers of approximately 0.04 eV to change the output values from 0 to 1, and energy barriers of approximately 0.10 eV to change the output values from 1 to 0.

5.2. Stability plots

To confirm the stable operation of the single-electron CCN gate, its stability plot has been constructed. The stability plot of a single-electron circuit with n inputs is an n-dimensional Cartesian space spanned by the n input voltages. Each point of this space corresponds to a combination of input voltage values. The free energy of the circuit is calculated at each point of the stability plot. Points that correspond to local minima of the circuit free energy are stable points (i.e. the corresponding combination of input voltage values prohibits electron tunnelling, keeping thus the electrons into the islands) and they are coloured white. On the other hand, points that correspond to local maxima of the circuit free energy are unstable points (i.e. the corresponding combination of input voltage values enhances electron tunnelling and the number of electrons into the islands cannot be determined) and they are coloured black. The rest of the points are coloured grey. Points near

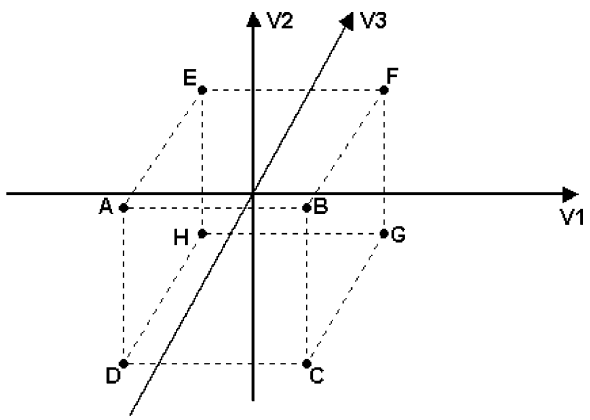

Fig. 6. The Cartesian space spanned by the three input voltages, and the three-dimensional stability plot of the gate with the eight operating points A–H.

Table 3
Stability plot points and input vectors

Operating point	$V1$ (mV)	$V2$ (mV)	$V3$ (mV)	Input vector
A	−60	105	−60	010
B	105	105	−60	110
C	105	−60	−60	100
D	−60	−60	−60	000
E	−60	105	105	011
F	105	105	105	111
G	105	−60	105	101
H	−60	−60	105	001

local free energy minima are coloured light grey, and the grey becomes darker as the energy of the points approaches local free energy maxima. Single-electron circuits must operate at stable, or at almost stable regions of the stability plot.

The stability plot of the single-electron CCN gate presented here is three-dimensional, and it is spanned by the three input voltages, as shown in Fig. 6. The points A–H of Fig. 6 represent the eight input combinations. It is reminded here that the input voltages can take only two values, −60 and 105 mV, which correspond to logic 0 and 1, respectively. There are eight possible combinations of the three input values, each of which corresponds to a point of the stability plot. Table 3 shows this correspondence.

The stability plot for the single-electron CCN gate has been obtained using SIMON. Fig. 7 shows two-dimensional sections of this plot. If $V3$ is constant and equal to −60 mV, the four possible combinations of the values of the other two inputs are represented by the points A, B, C, and D. If $V3$ is constant and equal to 105 mV, the four possible combinations of the values of the other two inputs are represented by the points E, F, G, and H. Fig. 7(a) shows the intersection of the stability plot with the plane *ABCD* of Fig. 6. Fig. 7(b) shows the intersection of the stability plot with the plane *EFGH* of Fig. 6. It is clear that all points A–H are located into stable regions, i.e. in white or light grey regions, which are stable enough to allow the desired operation of the circuit shown in Figs. 3 and 4.

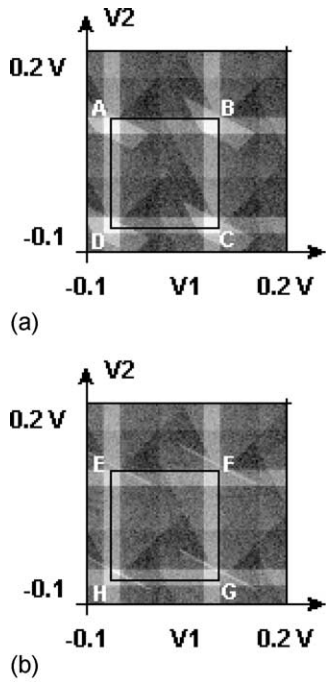

Fig. 7. Stability plots of the single-electron CCN gate, $V2$ versus $V1$, (a) $V3$ is constant and equal to −60 mV and (b) $V3$ is constant and equal to 105 mV.

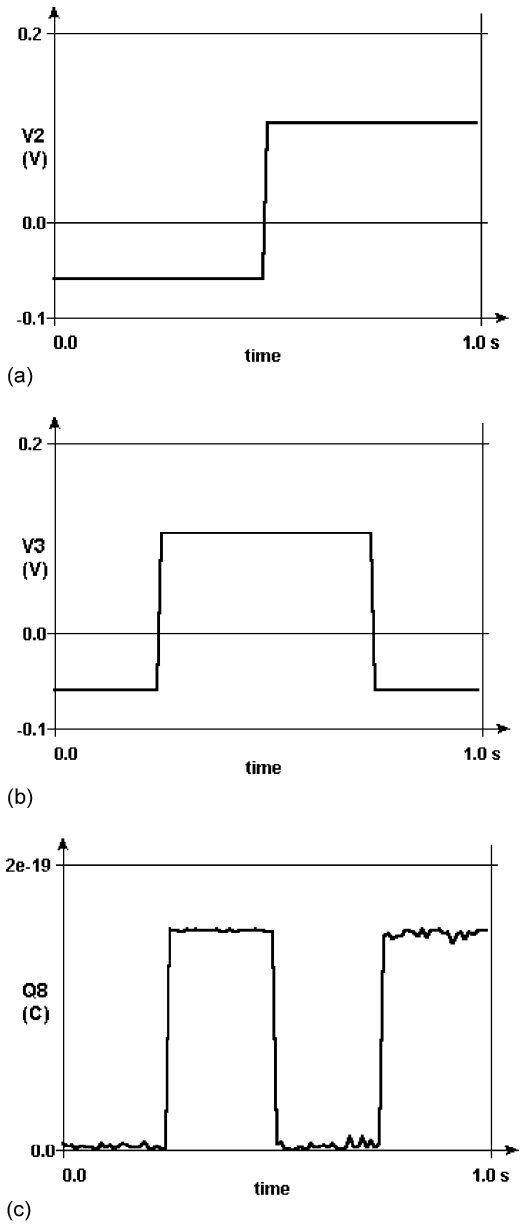

Fig. 8. Operation of the single-electron CCN gate as a XOR gate. (a) Time variation of the input voltage $V2$, (b) time variation of the input voltage $V3$ and (c) time variation of the charge in the output island $N8$.

6. Universality of the single-electron Control–Control-Not gate

The single-electron CCN gate is a universal gate. The CCN gate can operate as the logic gates XOR, AND, NAND and NOT by simply putting one or two of its inputs to a specific logic value.

6.1. XOR gate

The single-electron CCN gate can operate as a XOR gate either by keeping the first input to logic 1 or by keeping the second input to logic 1. The operating points of the XOR gate are B, C, E and G, if the first input is kept at logic 1, or

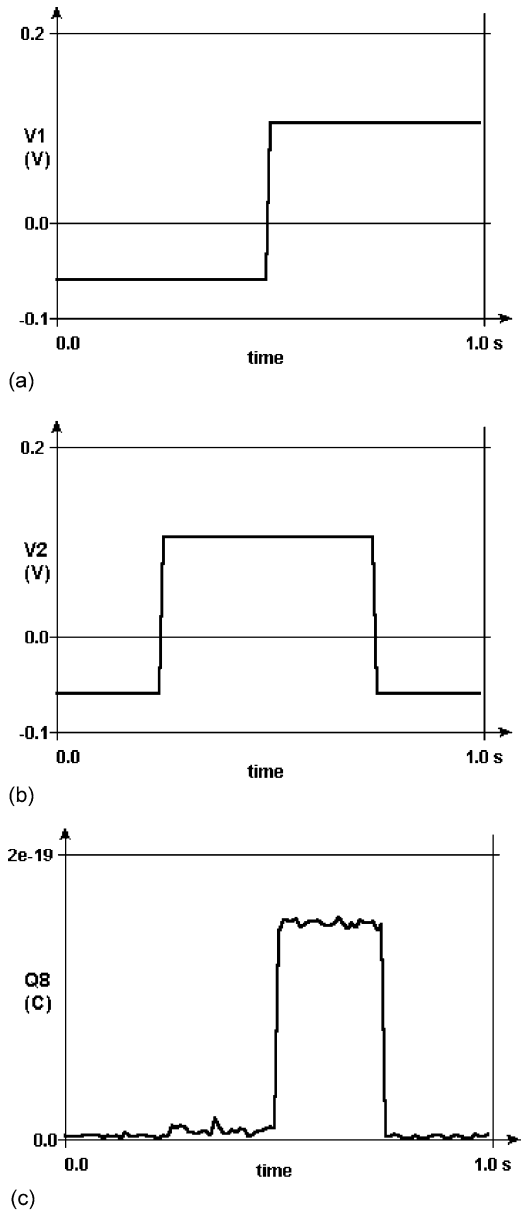

Fig. 9. Operation of the single-electron CCN gate as an AND gate. (a) Time variation of the input voltage $V1$, (b) time variation of the input voltage $V2$ and (c) time variation of the charge in the output island $N8$.

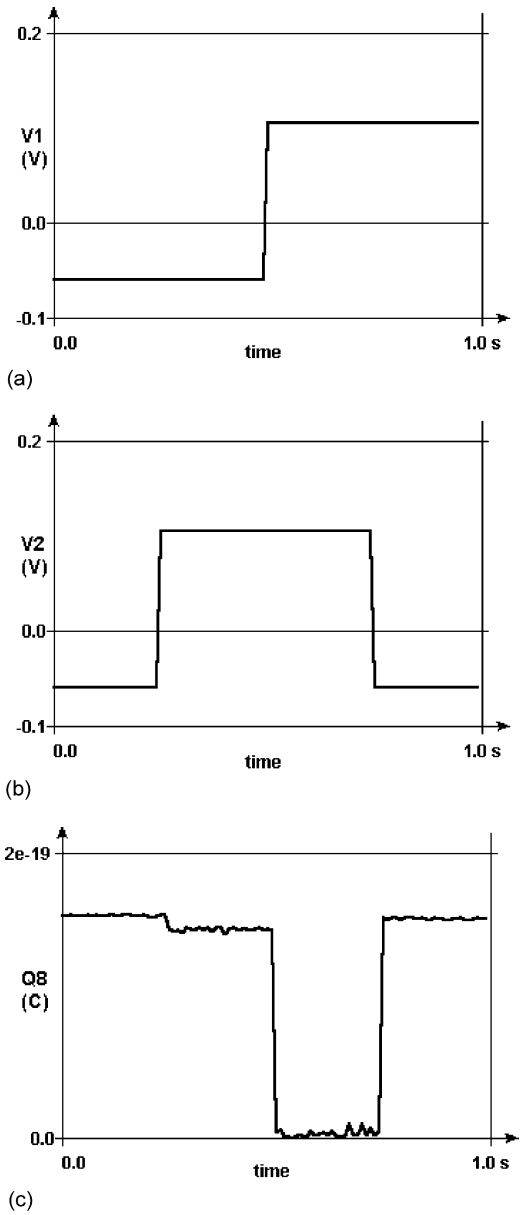

Fig. 10. Operation of the single-electron CCN gate as a NAND gate. (a) Time variation of the input voltage $V1$, (b) time variation of the input voltage $V2$ and (c) time variation of the charge in the output island $N8$.

A, B, E and F, if the second input is kept at logic 1. It is clear from Figs. 6 and 7 that the XOR operation of the gate is stable. Fig. 8(a) and (b) shows the time variation of the voltages $V2$ and $V3$, and Fig. 8(c) shows the time variation of the charge in the output island $N8$.

6.2. AND gate

The single-electron CCN gate can operate as an AND gate by keeping its third input to logic 0. The operating points of the AND gate are A–D, and the AND operation of the gate is stable. Fig. 9(a) and (b) shows the time variation of the voltages $V1$ and $V2$, and Fig. 9(c) shows the time variation of the charge in the output island $N8$.

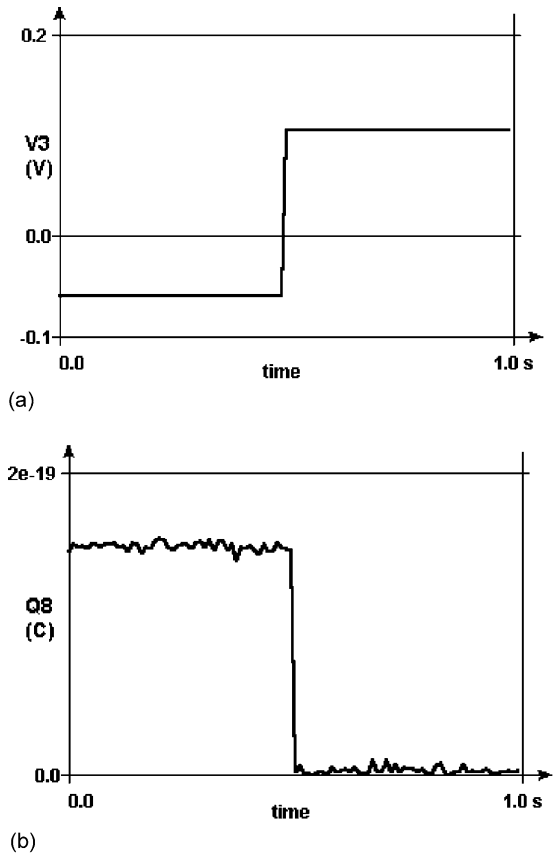

Fig. 11. Operation of the single-electron CCN gate as a NOT gate. (a) Time variation of the input voltage $V3$ and (b) time variation of the charge in the output island $N8$.

6.3. NAND gate

The single-electron CCN gate can operate as a NAND gate by keeping its third input to logic 1. The operating points of the NAND gate are E–H, and the NAND operation of the gate is stable. Fig. 10(a) and (b) shows the time variation of the voltages $V1$ and $V2$, and Fig. 10(c) shows the time variation of the charge in the output island $N8$.

6.4. NOT gate

The single-electron CCN gate can operate as a NOT gate by keeping its first and second inputs to logic 1. The operating points of the NOT gate are B and F, and the NOT operation of the gate is stable. Fig. 11(a) shows the time variation of the voltage $V3$, and Fig. 11(b) shows the time variation of the charge in the output island $N8$.

7. Conclusions

The single-electron universal CCN gate is possible. Single-electron digital circuits can be constructed using only this universal gate with obvious fabrication advantages. The free energy history diagrams and stability plots show that the single-electron CCN gate presented in this paper is stable. Simulation showed that the proposed single-electron CCN gate is universal and it can operate as a XOR, AND, NAND, or NOT gate at stable regions. The proposed gate comprises only eight islands, 12 junctions and five capacitors and it is therefore expected to occupy reasonably small chip area.

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