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A single-electron three-input AND gate

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Abstract

The design of a single-electron AND gate with three inputs is presented for the first time in this paper. The operation of this gate has been simulated using a well-known single-electron circuit simulator. Furthermore, the stability of its operation has been studied by constructing the free-energy history diagram, and by constructing and analyzing the corresponding three-dimensional stability plot, using Monte Carlo simulation. Simulation has verified the correct and stable operation of the gate. © 2002 Elsevier Science Ltd. All rights reserved.

Keywords: Single-electron circuits; Logic gates; Nanoelectronics

1. Introduction

The microelectronics industry has charted a path into the age of sub-100 nm manufacturing, in order to maintain the rate of miniaturization (often referred to as 'Moore's law') which powered-up its development until now [1]. As the dimensions of the integrated circuits are pushed down into the nanometer regime, the limitations of the MOSFET device become more and more apparent [2]. One of the most important limitations is the electron tunneling through gate oxide, and research is currently conducted for the fabrication of new gate dielectrics [3,4]. Two of the most promising emerging nanoelectronic technologies are quantum cellular automata [5–7] and single-electronics [8]. Single-electronics is a technology that makes possible the control of transport and position of a single electron or a small number of electrons. Single-electronics may lead to a new generation of very fast processors with small power consumption. The fundamental physical principle of single-electronics is the Coulomb blockade, which has been observed and studied by Gorter [9]. Since then single-electronics has received increasing attention because of the possibility of producing circuits that combine large integration and low power dissipation [8,10].

Several single-electron circuits have been recently proposed in the literature: single-electron memories [11–15], inverters [16,17], pumps [16,17], majority gates [18,19], and logic gates [20,21]. The need for computer-aided design and simulation of single-electron circuits has long been recognized [22]. Several simulators have been implemented to support single-electron circuit design [23–27].

A single-electron three-input AND gate is presented for the first time in this paper. The gate comprises five tunnel junctions, three capacitors and four islands, and has been designed and simulated using SIMON. SIMON is based on a Monte Carlo method [27]. The operation of this gate was simulated and its correct logical operation has been verified. Furthermore, the stability of its operation has been studied by constructing the free-energy history diagram, and by constructing and analyzing the corresponding three-dimensional stability plot. It has been shown that the gate operation is stable.

2. Single-electron circuits

Single-electron circuits consist of conducting islands, tunnel junctions, capacitors, and voltage sources. The islands are arbitrarily connected with tunnel junctions, capacitors and voltage sources. The basic principle of single-electronics is that one needs Coulomb energy E_c to charge an island with an electron. This energy is

$$E_c = \frac{e^2}{2C_i} \tag{1}$$

where C_i is the capacitance of the island and e the elementary electronic charge. Electrons tunnel independently from island to island through tunnel junctions. To assure that electron states are localized on islands, all tunnel resistances

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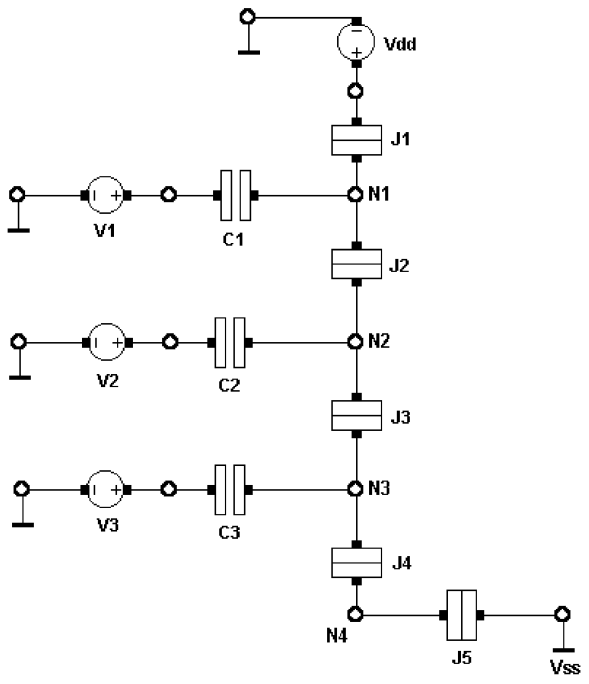

Fig. 1. The single-electron three-input AND gate.

must be larger than the fundamental resistance R_q:

$$R > R_q = \frac{h}{e^2} \cong 25,813\ \Omega \tag{2}$$

where h is Planck's constant.

To simulate the tunneling of electrons from island to island in a single-electron circuit one has to determine the rates of all possible tunnel events. The tunnel rate of a possible tunnel event depends on the change in the circuit's free energy caused by this particular event [8,26]. The free energy, F, of a single-electron circuit is the difference of the electrostatic energy, U, stored in its capacitances and the work done by the voltage sources of the circuit, W:

$$F = U - W \tag{3}$$

The electrostatic energy is given by

$$U = \frac{1}{2}(q, v)\begin{pmatrix} V \\ Q \end{pmatrix} \tag{4}$$

where, q and v are the unknown parts of the island charge and voltage matrices, respectively, and Q and V are the known parts of the island charge and voltage matrices, respectively. The work done by the voltage sources is given by

$$W = \sum_n \int V_n(t) i_n(t) \mathrm{d}t \tag{5}$$

where $V_n(t)$ is the voltage of the nth voltage source, and $i_n(t)$ is the current through the nth voltage source.

The tunnel rate, Γ, for a particular tunnel event is given by

$$\Gamma = \frac{\Delta F}{e^2 R_T\left(1 - \exp\left(-\frac{\Delta F}{kT}\right)\right)} \tag{6}$$

where ΔF is the change in free energy caused by this particular tunnel event, R_T is the tunnel resistance of the tunnel junction through which the electron is transported, and kT is the thermal energy (k is Boltzmann's constant, and T the temperature). Once the tunnel rates for all possible tunnel events are known, the actually occurring event is determined using a Monte Carlo method combined with an exponential distribution of tunnel events [17]. The time duration of a particular tunnel event is given by

$$\Delta t = -\frac{\ln(r)}{\Gamma} \tag{7}$$

where r is an evenly distributed random number in the interval [0,1]. Among all possible tunnel events, the event with the shortest time duration takes place [8,26].

3. The single-electron three-input AND gate

The single-electron three-input AND gate is shown in Fig. 1. The circuit comprises four islands, N1–N4, bounded by five tunnel junctions J1–J5 and three capacitors C1–C3. The tunnel junctions J1, J2, J3 and J4 are identical. The resistance of each one of these junctions is $10^5\ \Omega$ and the capacitance 10^{-18} F. Tunnel junction J5 is less transparent, in order to prevent electron transport from the ground (Vss) to island N4 and vice versa. Its resistance and capacitance are $10^7\ \Omega$ and 10^{-18} F, respectively. The voltage Vdd is constant and its value is 0.115 V.

$V1$, $V2$ and $V3$ are the inputs to the AND gate and can take only two values, −0.1 V, which corresponds to the logic '1', and 0.1 V, which corresponds to the logic '0'. The input voltages are applied to the corresponding nodes through the capacitors C1, C2 and C3. These capacitors are identical, and their capacitance is 10^{-18} F. The gate output is island N4. The presence of a positive charge on this island corresponds to the logic '1', whereas the absence of positive charge corresponds to the logic '0'.

The simulation of the gate operation is shown in Fig. 2. Fig. 2(a)–(c) show the time variation of input voltages $V1$, $V2$ and $V3$, respectively. The inputs are piece-wise constant, and apply all possible combinations of logic '0' and '1' to the gate. Fig. 2(d) shows the time variation of the charge at the output node N4. The charge at N4 is positive only when the input vector [111] is applied, and it is zero, when any other input vector is applied. The output transition from logic '0' to logic '1' and vice versa does not drive the gate to instability.

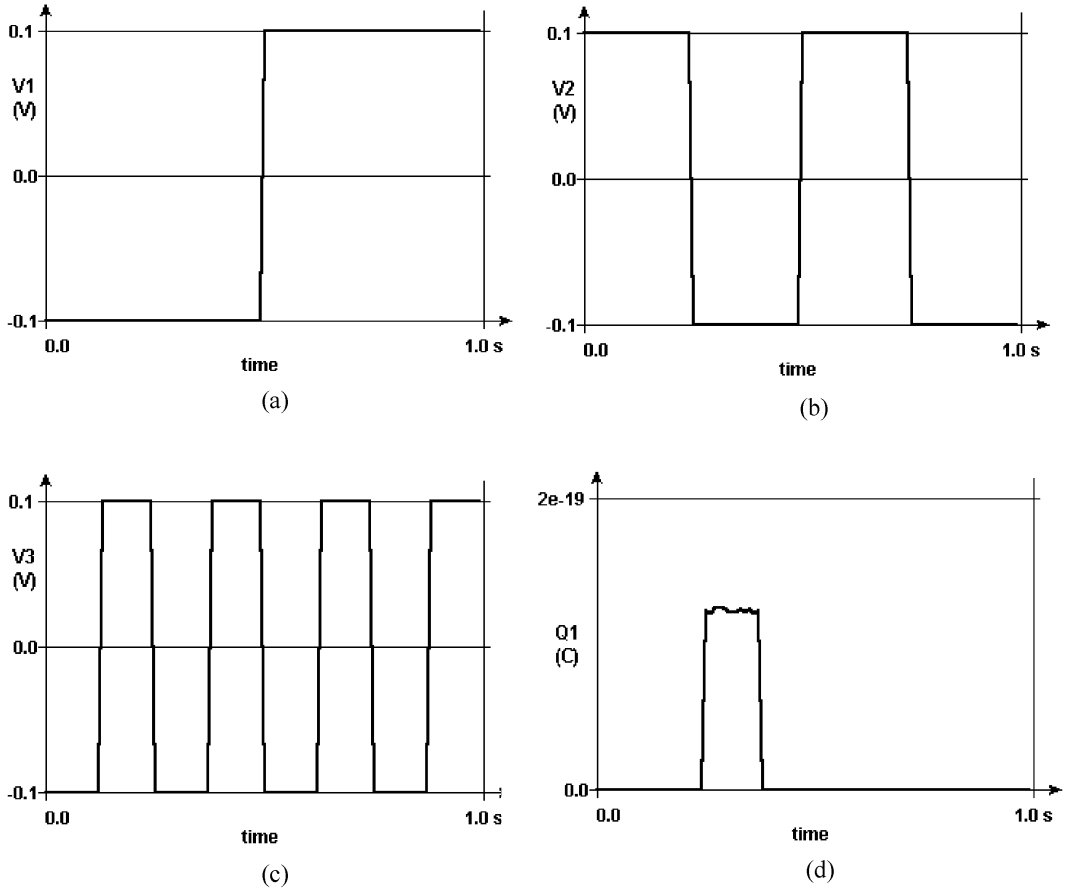

Fig. 2. The operation of three-input AND gate. (a), (b) and (c) time variation of input voltages *V*1, *V*2 and *V*3, respectively. (d) Time variation of the charge at the output node N4.

4. Stability of the gate operation

SIMON provides the possibility to calculate the current in the branches of the circuit. Such a calculation has been carried out and showed that during the output transition from logic '0' to logic '1' an electron is transported from node N4 to Vdd, through junctions J4, J3, J2, and J1. The change in the circuit's free energy during the output transition from '0' to '1' has been calculated and the circuit's free energy history is shown in Fig. 3.

During the first time step (0 to 1 on the *x*-axis of Fig. 3), it is assumed that any one of the seven input vectors [000], [001], [010], [011], [100], [101], or [110] is applied to the gate. In this case the output is '0', i.e. no positive charge is present at N4. During the second time step (1 to 2 on the *x*-axis), an electron is transported from N4 to N3 through J4 and the free energy increases. During the third time step, the electron is transported from N3 to N2 through J3 and the free energy decreases slightly. During the fourth time step, the electron is transported from N2 to N1 through J2 and the free energy increases again. Finally, during the fifth time step, the electron is transported from N1 to Vdd through J1, leaving a positive charge on the output node N4, and the free energy decreases significantly. Fig. 3 shows that when the output is at logic '1', the free energy of the circuit is less than its free energy when the output is at logic '0'. Furthermore, the free energy history diagram showed that there are two energy minima, corresponding to outputs '0' and '1'. For output transitions from '0' to '1' and vice versa, an

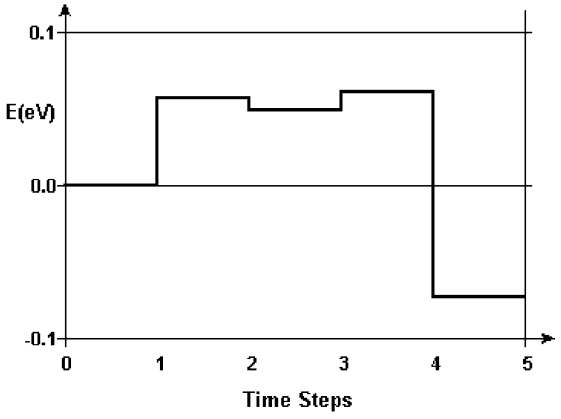

Fig. 3. Free energy history of the circuit for the output transition from '0' to '1'.

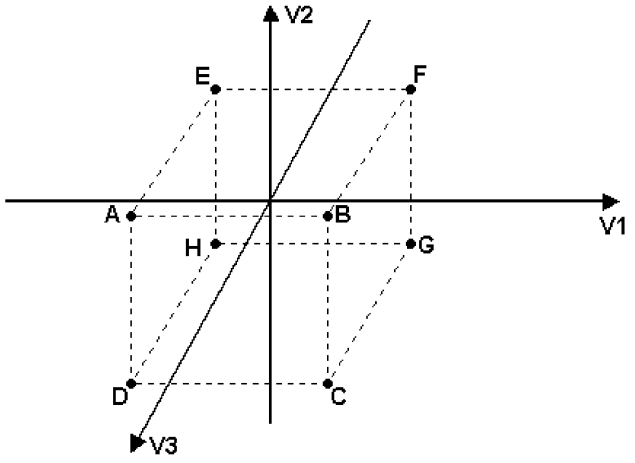

Fig. 4. The Cartesian space created by the three input voltages and the three-dimensional stability plot of the gate, with the eight operating points *A*, *B*, *C*, *D*, *E*, *F*, *G* and *H*.

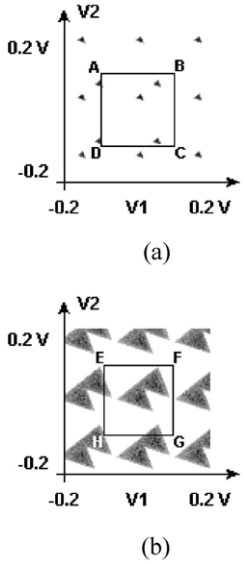

Fig. 5. The stability plot of the three-input AND gate for the inputs *V*1–*V*2: (a) with $V3 = 0.1$ V and (b) with $V3 = -0.1$ V. White regions are stable regions whereas gray regions are unstable regions. Any operating point corresponds to one corner of the squares.

energy barrier, shown in Fig. 3 between the values 1 and 4 along the *x*-axis, has to be surmounted. This is a strong indication of the stable operation of the three-input AND gate.

To confirm the stable operation of the gate, its stability plot has been constructed. The stability plot of a single-electron circuit with *n* inputs is an *n*-dimensional Cartesian space spanned by the *n* input voltages. Each point of this space corresponds to a combination of input voltage values. The free energy of the circuit is calculated at each point of the stability plot. Points that correspond to local minima of the circuit free energy are stable points (i.e. the corresponding combination of input voltage values prohibits electron tunneling, thus, keeping the electrons into the islands) and are colored white. On the other hand, points that correspond to local maxima of the circuit free energy are unstable points (i.e. the corresponding combination of input voltage values enhances electron tunneling and the number of electrons into the islands cannot be determined) and are colored black. The rest of the points are colored gray. Points near local free energy minima are colored light gray, and the gray becomes darker as the energy of the points approaches local free energy maxima. Single-electron circuits must operate at stable or at almost stable regions of the stability plot.

The stability plot of the three-input AND gate presented here is three-dimensional, and it is spanned by the three input voltages, as shown in Fig. 4. It is reminded here that the input voltages can take only two values −0.1 and 0.1 V, which correspond to logic '1' and '0', respectively. There are eight possible combinations of the input values, each of which corresponds to a point of the stability plot. Table 1 shows this correspondence.

Table 1

Stability plot points	*V*1	*V*2	*V*3	Input vectors
A	−0.1	0.1	0.1	100
B	0.1	0.1	0.1	000
C	0.1	−0.1	0.1	010
D	−0.1	−0.1	0.1	110
E	−0.1	0.1	−0.1	101
F	0.1	0.1	−0.1	001
G	0.1	−0.1	−0.1	011
H	−0.1	−0.1	−0.1	111

The calculated stability plot for the three-input AND gate has been obtained using SIMON. Fig. 5 shows two-dimensional sections of this plot. Fig. 5(a) shows the intersection of the stability plot with the plane *ABCD* of Fig. 4. It is clear that the points *A*, *B*, *C* and *D*, which represent four of the eight input combinations, are located in the stable regions. Fig. 5(b) shows the intersection of the stability plot with the plane *EFGH* of Fig. 4. It is clear that the points *E*, *F*, *G* and *H*, which represent the other four of the eight input combinations, are also located in the stable regions.

5. Conclusions

A single-electron three-input AND gate was presented in this paper. The gate executes the logic AND operation with three inputs and has been designed and simulated using SIMON. The gate comprises five tunnel junctions, three capacitors and four islands. The output is an island and the presence of a positive charge on it corresponds to the logic '1', whereas the absence of positive charge corresponds to the logic '0'. The energy history diagram and the stability plot showed that the gate operates in stable regions.

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